ABSTRACT OF THE DISCLOSURE

The present invention is a method and apparatus whereby two NMOS or PMOS devices connected in series in a stacked gate configuration formed on SOI exhibit improved ESD response characteristics. The shared source-drain region between the two devices is formed to have a dopant depth in the shared region that does not extend through the silicon layer to the BOX layer. This provides a common body for the two devices, and thus a single parasitic bipolar transistor is formed between the drain of one NMOS or PMOS device and the source of the second NMOS or PMOS device. Simultaneous snapback occurs for the two devices through the common body. A further embodiment includes a method of forming two or more stacked gate NMOS or PMOS devices on SOI. The method includes protecting the shared source-drain region between two NMOS or PMOS devices during a final doping step and silicide processing.